Advantages of ISP-Based PLDs over Traditional PLDs

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Introduction

As time-to-market pressures increase, design engineers continually look for ways to advance the development of system-level products and ensure problem-free manufacturing. Programmable logic devices (PLDs) that support in-system programmability (ISP) can help accelerate development time, simplify manufacturing flow, lower inventory costs, and improve printed circuit board (PCB) testing capabilities.

This product information bulletin discusses the advantages of ISP-capable PLDs over traditional PLDs (i.e., PLDs without ISP capability).

Development

Traditional PLDs require the use of development sockets, which add additional cost and can increase signal path loading in a system. ISP-capable PLDs, however, eliminate the need for development sockets because they are soldered directly to the PCB. During the development stage, the designer can quickly make changes to on-board ISP-capable devices, which shortens the design cycle and reduces the likelihood of damage caused by extensive handling. The designer can save even more time by using a programming interface that can program multiple devices simultaneously.

After the development stage, the designer can use the same ISP-capable device for production. Thus, the board design can be laid out and fabricated before the PLD design is complete. Because the designer can work on the board layout and logic design simultaneously, the design/layout time is shortened, resulting in faster time-to-market. Designers using ISP-capable devices have reduced their design cycle time up to 50% when compared to traditional PLDs.

Unlike ISP-capable PLDs, traditional PLDs may require a stand-alone PLD programmer (typically costing $3,000 to $5,000) for device programming. These traditional PLDs have stand-alone programming steps that require extensive device handling, which increases the likelihood of electrostatic discharge (ESD) damage and bent leads. In addition, the extra steps lengthen and complicate the production cycle.

Altera® ISP-capable PLDs allow designers to solder blank devices directly to the PCB, and then program and reprogram the devices during the development cycle. The Altera MAX+PLUS® II development software maintains the pin-outs when changes are made to the logic. By maintaining pin-outs, the MAX+PLUS II software helps eliminate the need for PCB respins and allows the board to be manufactured early in the development cycle, reducing the overall time-to-market and design costs.

Table 1 compares the development issues of ISP-capable PLDs vs. traditional PLDs.

Table 1. Development Issues of ISP-Capable PLDs vs. Traditional PLDs

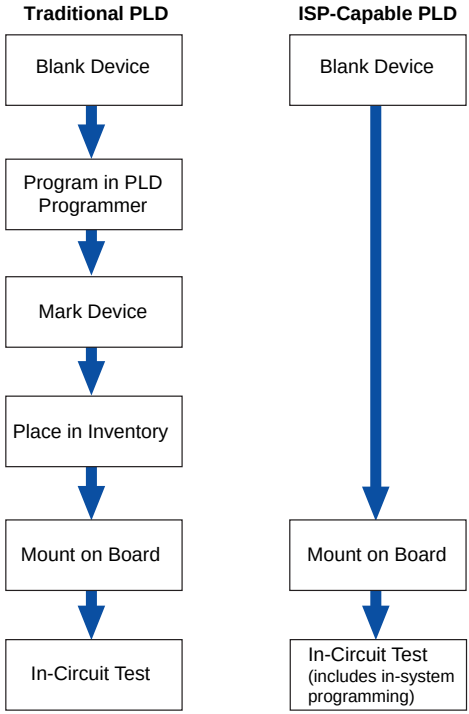
Issue	ISP-Capable PLDs	Traditional PLDs
Development socket		✓
Stand-alone PLD programmer		✓
Possible board respin after development		✓
Fast time-to-market	✓	✓

Manufacturing

Device programming with ISP-capable devices, performed just before board test, fits into the standard manufacturing flow. In fact, incorporating ISP-capable devices into the manufacturing flow provides significant financial incentive. Eliminating a dedicated programming step in the manufacturing process and combining the step with the board-test function improves manufacturing efficiency and helps the manufacturing engineer increase throughput. Because design revisions do not waste devices or require reprogramming or relabeling, using ISP-capable devices results in a high manufacturing yield. Reducing manufacturing steps also save time and result in fewer mistakes.

ISP-capable PLDs also reduce costs and quality problems that can arise from bent leads, poor soldering, ESD, and misplaced devices or device programs on the board. Programming ISP-capable PLDs directly on the PCB can reduce coplanarity and bent lead problems in devices with fragile packages (e.g., 100-pin thin-quad flat pack (TQFP) packages). Reducing handling and quality problems allow higher PCB yields from the manufacturing process. Figure 1 shows how ISP-capable PLDs simplify the manufacturing process compared to traditional PLDs.

Figure 1. ISP-Capable PLDs vs. Traditional PLDs Manufacturing Flow



Inventory

Because traditional PLDs are programmed and marked prior to PCB assembly, the devices must be programmed, marked, and stored in inventory until they are ready for assembly. When using ISP-capable PLDs, PLDs are stored blank until they are ready to be programmed. ISP-capable PLDs may reduce PLD inventories by up to 50%, providing lower inventory costs. Table 2 compares the inventory processes of ISP-capable PLDs vs. traditional PLDs.

Table 2. Inventory Processes of ISP-Capable PLDs vs. Traditional PLDs

Issue	ISP-Capable PLDs	Traditional PLDs
Separate device inventories needed		✓
Must mark device before programming		✓
Possibility of remarking		✓
Possibility of board inventory rework		✓
Inventory reduction	✓	

IEEE 1149.1 (JTAG) Boundary-Scan Support

In the 1980s, the Joint Test Action Group (JTAG) developed the IEEE 1149.1-1990 specification for boundary-scan testing. The boundary-scan test (BST) architecture offers the capability to efficiently test devices on PCBs with tight lead spacing (not all ISP-capable PLDs support JTAG). JTAG allows manufacturing engineers to use in-circuit testers for PLD programming, which improves the manufacturing process by eliminating the cost of a separate programming station, reducing the number of manufacturing steps, and allowing for reduced handling of the devices.

Implementing ISP through the JTAG test port allows programming to be easily completed on manufacturing in-circuit testers. JTAG can be used for both programming and testing by using the four-wire Test Access Port (TAP) along with some associated software to transfer necessary data. To speed up programming, the devices can be connected to the same JTAG port. In addition, some PLDs can be programmed concurrently. If the PCB contains many boards that need programming and testing, concurrent programming can save a significant amount of time and money. PLDs that use proprietary programming techniques may not support concurrent programming and may require a different setup and additional hardware for testing. Table 3 compares the JTAG implementation of ISP-capable PLDs to that of traditional PLDs.

Table 3. JTAG Implementation of ISP-Capable PLDs vs. Traditional PLDs

Issue	ISP-Capable PLDs	Traditional PLDs
Coplanarity problems		✓
Bent leads		✓
Stand-alone programming required		✓
Ability to increase throughput	✓	
Ability to increase yields	✓	
Supports JTAG programming	✓	

In-Field Upgrades

With ISP, designers can easily maintain and upgrade ISP-capable devices, allowing them to fix mistakes, add additional functions and features, and make changes to accommodate a new standard. These features offer tremendous money and time savings because system upgrades can be performed in the field. The end user also benefits because design changes can be downloaded to the system in the field via a download cable or an embedded processor, and ISP-capable PLDs can be reprogrammed while installed in the system. This process simplifies implementation of code revisions and technical modifications in the field. Additionally, inexpensive in-field upgrades allow early product release, because final designs can be directly loaded into a system in the field.

Second-Time Fitting

ISP-capable PLDs that have good second-time fitting can accommodate design changes when device pin assignments remain fixed. This ability to retain pin-outs and maintain performance ensures that the PCB design can be isolated from the programmable logic design and allows the PCB to be manufactured early in the design cycle.

Vertical Migration

ISP-capable devices that support vertical migration give the designers additional flexibility after the PCB is complete. You can save cost during production if less expensive devices are used. With vertical migration designers can substitute a smaller density ISP-capable device after development is completed, allowing for cost savings during production. Vertical migration also gives designers the flexibility to migrate to devices that offer higher performance.

Tables 4, 5, and 6 show the Altera MAX® 9000 (including MAX 9000A), MAX 7000S, and MAX 7000A devices that support vertical migration.

Table 4. MAX 9000 Device Vertical Migration Capability

Device	Fastest t_{PD} (ns)	84-Pin PLCC	208-Pin RQFP	240-Pin RQFP	280-Pin PGA	304-Pin RQFP	356-Pin BGA
EPM9320	15	✓	✓		✓		✓
EPM9320A	7.5	✓	✓				✓
EPM9400	15		✓	✓			
EPM9480	15		✓	✓			
EPM9480A	10		✓	✓			
EPM9560	15		✓	✓	✓	✓	✓
EPM9560A	10		✓	✓			✓

Table 5. MAX 7000S Device Vertical Migration Capability

Device	Fastest t_{PD} (ns)	44-Pin PLCC, *Note (1)*	44-Pin TQFP, *Note (1)*	84-Pin PLCC, *Note (1)*	100-Pin PQFP	100-Pin TQFP, *Note (1)*	160-Pin PQFP	208-Pin PQFP, *Note (1)*
EPM7032S	6	✓	✓					
EPM7064S	5	✓	✓	✓		✓		
EPM7128S	6			✓	✓	✓	✓	
EPM7160S	7.5			✓		✓	✓	
EPM7192S	7.5							
EPM7256S	7.5							✓

Note:
(1) This MAX 7000S device package supports vertical migration with other MAX 7000A devices.

Table 6. MAX 7000A Device Vertical Migration Capability

Device	Fastest t_{PD} (ns)	44-Pin PLCC, *Note (1)*	44-Pin TQFP, *Note (1)*	84-Pin PLCC, *Note (1)*	100-Pin TQFP, *Note (1)*	144-Pin TQFP	208-Pin PQFP, *Note (1)*	256-Pin BGA
EPM7032A	5.0	✓	✓					
EPM7064A	5.0	✓	✓	✓	✓			
EPM7128A	5.0			✓	✓	✓		
EPM7256A	6.0				✓	✓	✓	✓
EPM7384A	7.5					✓	✓	✓
EPM7512A	7.5					✓	✓	✓
EPM71024A	7.5						✓	✓

Note:
(1) This MAX 7000A device package supports vertical migration with other MAX 7000S devices.

Program/Erase Cycles

The number of program/erase cycles offered by ISP-capable devices varies by vendor. Usually, 100 program/erase cycles are sufficient for designs using ISP-capable devices. For applications requiring more than 100 program/erase cycles, designers should use FLEX® 10K or FLEX 8000 devices, which can be reconfigured an unlimited number of times.

Conclusion

ISP-capable devices offer designers many advantages over traditional PLDs. ISP-capable devices allow designers to achieve cost reductions in their design development and allow manufacturing engineers to increase throughput and yield during production. Additionally, in-field upgrades are simplified and are much more cost-effective and practical than with traditional PLDs. Thus, ISP-capable PLDs should be used to ensure fast time-to-market as well as low cost.

Reference

Conner, Doug. "In-System Programmable Logic Simplifies Prototyping to Production." *EDN Magazine*, September 16, 1996, pg. 38.